REMARKS

Claims 1-10, 19, and 20 are all the claims presently pending in the application. Claims 11-18 are withdrawn but subject to rejoinder.

It is noted that the claim amendments, if any, are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 19 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,869,844 to Liu et al. Claims 1-6 and 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu, further in view of US Patent 6,329,391 to Finzi.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu, further in view of US Patent 6,815,771 to Kimura. Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu/Finzi, further in view of Kimura.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to an electronic chip including a first circuit design module having a first grid and a second circuit design module having a second grid. The first grid and the second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in the fabrication.

As explained beginning at paragraph [0039], the conventional practice in SOI circuit design and fabrication is that the various circuit design modules are interconnected in the final metallization step (e.g., M5).

The claimed invention, on the other hand, teaches that the charging due to plasma processing is not distributed uniformly over the two-dimensional surface of the chip. Therefore, the plasma processing can cause differential voltages across the chip, including, particularly, differential voltages between the grids of the various design modules on the chip. To preclude

this differential voltage condition, the present invention teaches that the design modules should be interconnected prior to the final metallization that is taught by conventional wisdom.

II. THE PRIOR ART REJECTIONS

The examiner alleges that Liu anticipates claim 19, and, when modified by Finzi, renders obvious claims 1-6 and 8-10, and when modified by Kimura, renders obvious claim 20. The Examiner also alleges that further modification of Liu/Finzi by Kimura renders obvious claim 7.

Applicants again respectfully disagree, since it is again pointed out that the present invention teaches that a different problem is causing the problem, thereby the environment of these two references fails to satisfy the plain meaning of the claim language of the independent claim.

More specifically, as explained in paragraph [0037], the present invention teaches that the damage to the chip components is due to two-dimensional differences in charging during the plasma process, so that, as shown in figure 2, different surfaces of the chip will receive different amount of charges. Moreover, as explained in paragraph [0032] and illustrated in Figure 3, the present invention exemplarily defined by independent claim 19 is directed toward a chip 300 that has a plurality of grids resultant from respective design efforts of different engineering teams. These design grids might typically be power or ground grids, as described in dependent claims 3, 13. When these design grids are sufficiently large on chips, such as SOI (e.g., see paragraph [0036] and dependent claims 6, 7, 15, 16, and 20), that have a layer isolating the circuit layers from the substrate, the inventors have surmised that the reason for failures during fabrication is due to lateral differences in charging during plasma processing that shows up in these different design team grids.

Therefore, the present invention teaches that, to overcome the damage done by this unequal distribution of charges, the different grids of different design modules should be electrically interconnected before the first plasma operation after the grid has been formed. If these grids are not interconnected, as explained above, the plasma process can provide a different distribution of charges on the different grids, thereby causing a differential voltage between the grids and potential damage to the circuits.

Primary reference Liu does not address chips having circuits isolated from the substrate, such as SOI, and the mechanism in this reference is based upon providing a discharge path from a protected structure through a back-to-back diode connected in series to the substrate, as clearly described in lines 14-15 of column 2 and lines 27-29 of column 3.

Therefore, relative to claim 19, the primary reference fails to satisfy the plain meaning of the claim language, since the only protective mechanism in Liu is to the substrate and involves only the gates, as shown in Figure 2. There is no mechanism that protects against a differential accumulation of charges across two grids that are isolated from the substrate, since the mechanism in Liu will inherently discharge to the substrate before a differential charge between the grids builds up. Stately slightly differently, the protective mechanism in Liu is only for the second grid 12 but not for the first grid 14, and that protective mechanism discharges to the substrate. There is no electrical interconnection between grids 12 and 14 in Liu.

Moreover, it is noted that dependent claim 20 specifically describes the chip as SOI. In the rejection, the Examiner attempts to modify the technique in primary reference Liu for the non-SOI structure to incorporate the SOI structure of Kimura and alleges that one would be motivated to "... *incorporate the teachings of Kimura into the device of Liu in order to have said chip including a silicon on insulator (SOI) structure to alleviate the problem of breakdown voltage.*"

However, Applicants submit that modification of Liu to convert it into SOI would change the underlying principle of operation of its protective mechanism, since this mechanism requires a path to the substrate, and SOI would preclude such path. Therefore, such conversion would be improper since it would defeat the purpose of the mechanism in the primary reference.

Thus, Applicants submit that the rejections for claims 19 and 20 fail to meet the initial burden for a *prima facie* rejection for at least two reasons. First, relative to claim 19, absent some express indication in Liu, there is no reason to consider the NROM as anything except a completely homogenous electronic circuit, thereby precluding the requirement that different design teams are required, let alone separate design grids. The Examiner makes no attempt to demonstrate that there are two design modules in Liu and, in effect, simply ignores the plain meaning of the claim language. Therefore, relative to claim 19, there has been no demonstration of separate grids requiring protection from a differential accumulation of charges during plasma

processing, since, first, isolated grids designed by different design teams have not been demonstrated, and, second, the protective mechanism in Liu will discharge any charge only for one grid and that discharge will be to the substrate. The mechanism of the present invention does not have available the discharge to the substrate, since the two grids are isolated from the substrate in the SOI environment and it truly does electrically interconnect the two grids.

Relative to claim 20, the rejection of record improperly attempts to simply change the chip of primary reference Liu into an SOI chip, thereby clearly and improperly changing its principle of operation.

Finally, relative to the Examiner's refusal to provide patentable weight to " ... no later than a first metalization layer of said chip" and "... a plasma processing", Applicants submit that the claim wording does indeed define a structure that is detectable in the finished product and, therefore, is not processing designation, as alleged by the Examiner. That is, the finished product includes two or more design grids, and these grids will be electrically interconnected with an actual structure that will be observable by one having ordinary skill in the art. Moreover, to one having ordinary skill in the art, this structure can be determined as having been fabricated in a step prior to one in which a plasma processing might be used after the two or more design grids have been formed. Therefore, as such, this wording does indeed have patentable weight, since such structure can be detected by one having ordinary skill in the art in a potentially infringing device.

Hence, turning to the clear language of the claims, in Liu there is no teaching or suggestion of: " ... a first circuit design module having a first grid; a second circuit design module having a second grid; and means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip", as required by claim 19.

Relative to claim 20, there is no proper motivation to modify primary reference Liu, since the Examiner attempts to simply convert the non-SOI chip of Liu into an SOI chip. Such conversion would defeat the purpose of primary reference Liu, since Liu depends upon being able to discharge accumulated charges to its substrate, and SOI inherently insulates from the substrate, thereby interfering with the mechanism in Liu.

Therefore, claims 19 and 20 are clearly patentable over Liu.

Relative to the rejection for claims 1-6 and 8-10, the same deficiencies identified above for claims 19 and 20 apply equally well. Primary reference Liu is not an SOI structure and cannot be converted without changing its principle of operation and the principle of operation of its mechanism to provide a discharge path to the substrate. Moreover, as mentioned above, Liu has not been demonstrated as resultant from two design modules, as clearly required by the plain meaning of the claim language, and only one of the two grids identified in the rejection has a protection mechanism. There is no electrical interconnection between the two grids.

The Examiner does concede that Liu fails to demonstrate a mechanism to preclude an accumulation of charges and introduces secondary reference Finzi, alleging that it would have been obvious to modify Liu by Finzi "... *in order to have a protection circuit wherein two grids do not accumulates (sic) an excessive voltage due to the plasma process to improve a data speed.*"

Applicants submit that, to one having ordinary skill in the art, first, the technique in Finzi has nothing to do with improving data speed, and, second, primary reference Liu already has a breakdown mechanism to the substrate for one of its grids. Therefore, there would be no reason to modify Liu to provide a second breakdown mechanism to the substrate, and the rejection currently of record simply fails to meet the initial burden of a *prima facie* rejection since there is no reasonable motivation to modify the primary reference Liu.

Hence, relative to independent claim 1 and turning to the clear language of the claims, in Liu there is no teaching or suggestion of: "... a first circuit design module having a first grid; and a second circuit design module having a second grid, wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process."

Moreover, Applicants submit the following deficiencies in the rejection currently of record for the following dependent claims:

- relative to claim 6, the circuit in Liu is fabricated in the substrate, so that, in contrast to the SOI structure, there will inherently be substantial leakage of current in Liu;

- relative to claim 7, the further modification of the non-SOI structure of primary reference Liu changes the principle of operation of the circuit chip and the protective mechanism of Liu, since the circuit in Liu is fabricated on the substrate; and

- relative to claim 9, the Examiner is respectfully requested to identify the discussion in Liu that supports any concern about surface area.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Liu, Finzi, or Kimura, and the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-10, 19, and 20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Moreover, Applicants submit that claims 11-18 are subject to rejoinder and, therefore, also allowable, and Applicants request such rejoinder of claims.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

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Frederick E. Cooperrider
Registration No. 36,769

McGinn Intellectual Property Law Group, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (571) 273-8300 this Amendment under 37 CFR §1.116 to Examiner J. Im on September 25, 2006.

Frederick E. Cooperrider
Reg. No. 36,769